IN THE SPECIFICATION:

Please amend the second full paragraph on page 2 as follows:

State of the Art: Modern high-speed integrated circuit devices, such as synchronous dynamic random access memories (SDRAM), microprocessors, etc., rely upon clock signals to control the flow of commands, data, addresses, etc., into, through, and out of the devices. Additionally, new types of circuit architectures such as RAMBUS and ~~SLDRAM~~ synchronous link dynamic random access memory (SLDRAM) require individual parts to work in unison even though such parts may individually operate at different speeds. As a result, the ability to control the operation of a part through the generation of local clock signals has become increasingly more important. Conventionally, data transfer operations are initiated at the edges of the clock signals (i.e., transitions from high to low or low to high).

Please amend the third full paragraph on page 2 as follows:

In synchronous systems, integrated circuits are synchronized to a common system reference clock. This synchronization often cannot be achieved simply by distributing a single system clock to each of the integrated circuits for the following reason, among others. When an integrated circuit receives a system clock, the circuit often must condition the system clock before the circuit can use the clock. For example, the circuit may buffer the incoming system clock or may convert the incoming system clock from one voltage level to another. This processing introduces its own delay, with the result that the locally processed system clock often will no longer be adequately synchronized with the incoming system clock. The trend ~~towards~~ toward faster system clock speeds further aggravates this problem since faster clock speeds reduce the amount of delay, or clock skew, which can be tolerated.

Please amend the first full paragraph on page 3 as follows:

To remedy this problem, an additional circuit is conventionally used to synchronize the local clock to the system clock. Two common circuits which are used for this purpose are the phase-locked loop (PLL) and the delay-locked loop (DLL). In the phase-locked loop, a

voltage-controlled oscillator produces the local clock. The phases of the local clock and the system clock are compared by a phase-frequency detector, with the resulting error signal used to drive the voltage-controlled oscillator via a loop filter. The feedback via the loop filter phase locks the local clock to the system clock. The delay-locked loop generates a synchronized local clock by delaying the incoming system clock by an integer number of periods. More specifically, the buffers, voltage level converters, ~~etc.~~ etc., of the integrated circuit introduce a certain amount of delay. The delay-locked loop introduces an additional amount of delay such that the resulting local clock is synchronous with the incoming system clock.

Please amend the first full paragraph on page 4 as follows:

Figure 2 is a timing diagram for the synchronizing circuitry of Figure 1. As shown in Figure 2, the rising edge 26 of the XCLK signal 9, which is carried on the XCLK signal ~~line 6~~ line 8 of Figure 1, is aligned with the rising edge 28 of the DQ signal 25, which is carried on the DQ signal line 24 of Figure 1. As is indicated by the arrows shown in Figure 2, the rising edge 30 of DLLCLK signal 33 (carried on the DLLCLK signal line 32 of Figure 1) initiates the rise and fall of the DLLR signal 21 (carried on the DLLR signal line 20 of Figure 1), through the Rise Fall CLK Generator 18 (Figure 1), which in turn initiates the rising edge 28 of the DQ signal 25. Likewise, the rising edge 34 of the /DLLCLK signal 37 (carried on the /DLLCLK signal line 36) initiates the rise and fall of the DLLF signal 23 (carried on the DLLF signal line 22 of Figure 1), which in turn initiates the falling edge 42 of the DQ signal 25. For proper data synchronization, the timing difference 46 between the falling edge 44 of the XCLK signal 9 and the falling edge 42 of the DQ signal 25 must be less than the tAC specifications for the system in which the synchronizing circuitry will be used. For the example shown in Figure 2, the data is firing in a high-low, high-low pattern.

Please amend the first full paragraph on page 6 as follows:

The nature of the present ~~invention~~ invention, as well as other embodiments of the present ~~invention~~ invention, may be more clearly understood by reference to the following

detailed description of the invention, to the appended claims, and to several drawings herein, wherein:

Please amend the paragraph bridging pages 6 and 7 as follows:

Figure 3 is a block diagram of an embodiment of a data synchronizing circuit according to the present invention. The embodiment in Figure 3 includes a first phase detector 50, like the phase detectors known in prior art synchronizing circuitry, which detects the relative phases of the signal on the CLKIN signal line 52, a derivative of the signal on the system clock signal line XCLK 54, and the signal on the OUT_MDL signal line 56, which models the timing of the signal on the data output DQ signal line 58. In response to a timing difference between the relative phases of the signals on the CLKIN signal line 52 and the OUT_MDL signal line 56, the first phase detector 50 adjusts the delay to the signal on the CLKIN signal line 52 by sending shift left and shift right signals through respective ShiftL 60 and ShiftR 62 signal lines to the DLL delay elements 61 to phase-lock the respective rising edges 64 and 66 (Figure 4) of the CLKIN 53 and OUT_MDL 57 signals (Figure 4). Phase-locking the rising edges 64 and 66 (Figure 4) of the CLKIN 53 and OUT_MDL 57 ~~signals respectively~~ signals, respectively, causes the rising edges 68 and 70 (Figure 4) of the XCLK 55 and DQ 59 signals (Figure 4) to align.

Please amend the paragraph bridging pages 7 and 8 as follows:

Once the first phase detector 50 has achieved a phase-lock, it outputs a phase-lock signal through a phase-lock signal line 72 to initiate a second phase detector 74. The second phase detector 74 compares the relative phases of the signals on the /CLKIN signal line 76, which is a derivative of the signal on the /XCLK signal line 78, and the /OUT_MDL signal line 80, which models the inverse of the timing of the data ~~output~~ output DQ signal 59 on the DQ signal line 58. The CLKIN signal 53 and the XCLK signal 55 are related by a clock buffer 48. Similarly, the /CLKIN signal 77 and the /XCLK signal 79 are related by a clock buffer 49. In response to timing differences between the relative phases of the signals on the /CLKIN signal line 76 and the /OUT_MDL signal line 80, the second phase detector 74 adjusts the delay to the /DLLCLK

signal line 82, caused by a delay circuit 84 and within a predetermined range of variance, by sending a delay adjust control signal on a delay adjust signal line 86. Another delay circuit 88 delays the DLLCLK signal 91 on the DLLCK signal line 90 by a fixed amount selected by a set register circuit 92. Preferably, the set register circuit 92 sets the delay circuit 88 for the DLLCLK signal 91 on the DLLCLK signal line 90 in the middle of the delay range (e.g., set = ½ n where n is the integer number of delay elements). By placing the delay set in the middle of the delay range, the range of available positive and negative delays for the delay circuit 84 on the /DLLCLK signal line 82 is maximized. Alternatively, a third variable delay circuit could be used in place of delay circuit 88 to further fine-tune the rising edge of the system clock signal, though this is not preferred. Delaying the signal on the /DLLCLK signal line 82 by a variable amount controlled by the second phase detector 74 enables alignment of the rising edge 94 of the /CLKIN signal 77 with the rising edge 96 of the /OUT_MDL signal 81 (Figure 4). Alignment of the respective rising edges 94 and 96 of the /CLKIN 77 and /OUT_MDL 81 signals, in turn, results in the alignment of the respective falling edges 98 and 100 of the XCLK 55 and DQ 59 signals (Figure 4).

Please amend the first full paragraph on page 8 as follows:

As shown in Figure 4, by delaying the /DLLCLK signal 83 by a time interval necessary to align the falling edges 98 and 100 of the XCLK 55 and DQ 59 signals, the DLLF signal 103 on DLLF signal line 102, which is initiated by the rising edge 104 of the /DLLCLK signal 83, is delayed, resulting in a delay of the falling edge 100 of the DQ signal 59. With a second phase detector 74 and delay circuit 84, despite timing cycle dependant variations in delay elements affecting the primary clock signal adjustments through DLL delay elements 61, a signal which has been skewed to a 40/60 duty cycle from a 55/45 duty cycle may be corrected back to a 55/45 duty cycle for better performance at high speeds.

Please amend the paragraph bridging pages 8 and 9 as follows:

Figure 5 is a block diagram of an electronic system 200 which includes components having one or more substrates 206 comprising circuit traces or other signal lines and components configured according to one or more embodiments of the present invention. The electronic system 200 includes a processor 204 for performing various computing functions, such as executing specific software to perform specific calculations or tasks. Additionally, the electronic system 200 includes one or more input devices 208, such as a keyboard or a mouse, coupled to the processor 204 to allow an operator to interface with the electronic system 200. The electronic system 200 also includes one or more output devices 210 coupled to the processor 204, such output devices 210 including such outputs as a printer, a video terminal or a network connection. One or more data storage devices 212 are also conventionally coupled to the processor 204 to store or retrieve data from external storage media. Examples of conventional storage devices 212 include hard and floppy disks, tape cassettes, and compact disks. The processor 204 is also conventionally coupled to a cache memory 214, which is usually static random access memory ~~("SRAM"),~~ (SRAM) and coupled to DRAM 202. It will be understood, however, that the printed circuit board or other substrate 206 configured according to one or more of the embodiments of the present invention may be incorporated into any one of the cache, DRAM, input, output, storage and processor devices 214, 202, 208, 210, 212, and 204.

Please amend the first full paragraph on page 9 as follows:

As shown in Figure 6, circuitry 218, in accordance with one or more embodiments of the present invention described herein, may be fabricated on the surface of a semiconductor wafer 216 of silicon, gallium arsenide, or indium phosphide. One of ordinary skill in the art will understand how to adapt such designs for a specific chip architecture or semiconductor fabrication process. Of course, it should be understood that the circuitry 218 may be fabricated on semiconductor substrates other than a wafer, such as a Silicon-on-Insulator (SOI) substrate, a Silicon-on-Glass (SOG) substrate, ~~a Silicon-~~

~~on Sapphire~~ Silicon-on-Sapphire (SOS) substrate, or other semiconductor material layers on supporting substrates.